UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,633	06/27/2003	Rajeev Joshi	018865-004210US	8725

20350 7590 01/04/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,633	JOSHI ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The double patenting rejection of 15 September 2004 has been overcome.

Claim Objections

Claim 26 is objected to because of the following informalities: claim 26 is dependent on itself. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima et al., US Patent No. 5,723,900 in view of Hsuan, US Patent No. 6,429,509 B1.

Kojima teaches a method of making a chip device, the method comprising:

In fig. 2, providing a leadfame 12 that includes leads 16; providing a die 13 that includes a backside 13a, col. 3, lines 34-39,

coupling a frontside of the die to the leadframe with metal, with bumps 17, col. 4, lines 51-56; and in figs. 4H-J, encapsulating the die 14 with a body such that backside of the die is adjacent to a window defined within the body, over 13A.

limitations from claim 8, a method, in fig. 4F further comprising configuring the plurality of leads 16, col. 4, lines 47-50;

limitations from claim 16, the method, in fig. 4G, wherein the die is coupled to the leadframe via bumps, col. 4, lines 51-56;

limitations from claim 17, a method, in fig. 9, wherein the die is a first die, lower 13, and wherein the method includes attaching a second die, upper 13, to the leadframe, col. 6, lines 3-9.

Kojima does not specify forming an electrical terminal on the backside, but Hsuan does. Hsuan teaches in fig. 4I, wherein the backside of the die 430, forms an electrical terminal 410, col. 8, line 58 - col. 9 line 278, using solder bump, 415, col. 8, line 58 - col. 9 line 278, to bond and using reflowing, col. 7, lines 13-45;

limitations from claim 16, the method, wherein the die is coupled via solder, and wherein the solder bumps are reflowed, col. 7, lines 13-45;

limitations from claim 17, a method, in figs. 3C-3D, wherein the die is a first die 300(1) and wherein the method includes attaching a second die 300(2) to the surface;

Hsuan gives motivation on col. 3, lines 21-10. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Hsuan's invention with Kojima's invention would have been beneficial because it shortens the cycle time.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima in view of Hsuan as applied to claims 7, 8, 16, 17 above, and further in view of Maejima et al., U.S. Patent No. 5,347,709.

Kojima and Hsuan do not specify removing the resin flashing, but Maejima does. Maejima teaches a method, in fig. 14, further comprising removing dambars from the leadframe, removing mold flashes and resins from the leads, and solder plating the leads, col. 7, lines 44-63. Maejima gives motivation in col. 7, lines 44-63. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Maejima's process with Kojima's and Hsuan's invention would have been beneficial because the invention removes the negative bonding effects of the bonding.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima in view of Hsuan as applied to claims 7, 8, 16, 17 above, and further in view of Orso et al., U.S. Patent No. 6,018,686.

Kojima and Hsuan do not specify marking of the body on a surface opposite the window, but Orso does specify body marking. Orso teaches a method comprising

marking the body of the chip with a laser, and with ink, col. 1, lines 24-37. Orso gives motivation in col. 1, lines 24-37. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Orso's process with Kojima's and Hsuan's invention would have been beneficial because the invention gives indicia to dies which may be useful for sorting dies that pass inspection from those that do not pass.

Claims 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima in view of Hsuan as applied to claims 7, 8, 16, 17 above, and further in view of Layher et al., U.S. Patent No. 4,678,358.

Kojima and Hsuan do not specify using preplated leads, but Layher does. Layher teaches in figs. 1 and 2 forms lead frame 10 provided with preplated leads 11, p. 4, lines 25-41, and col. 2, line 47 - col. 3, line 10. Layher gives motivation in col. 2, lines 6-21. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Layher's process with Kojima's and Hsuan's invention would have been beneficial because the invention does not subject the parts to a working temperature that will diffuse or melt the coating.

The following rejection for claims 18-25 has been incorporated from the paper sent 15 September 2004 and is reiterated. Newly added claim 26 is further addressed:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18, 20, 24, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by McShane et al., U.S. Patent No. 5,147,821.

McShane anticipates a method of making a chip device, the method comprising: in fig. 1, providing a leadframe 16 that includes leads 20; providing a die 12 that includes a metallized backside 14; coupling the die to the leadframe,
and encapsulating the die with a body 22 such that, in fig. 4, the metallized backside of the die is adjacent a window defined within the body 56, col. 7, line 35-51;
in fig. 4, wherein the backside of the semiconductor die, covered by metallization 54, is exposed 56 through the window of the molding compound and wherein the backside is substantially flush with the exterior surface of the molding compound, wherein the thickness of 52 is heuristic and may be quite thin in addition to "substantially flush" being subjective to the observer, col. 7, line 35 - col. 8, line 10;

limitations from claim 20, in fig. 5, the method further comprising mounting a second semiconductor die, represented by A and B, including a second backside

to the leadframe, wherein second backside is exposed through a second window in the molding compound, 77 and 78, col. 8, lines 22-40;

limitations from claim 24, wherein ends of the leads are co-planar with the backside of the semiconductor die, in fig. 1, wherein the distal ends of leads 20 attached to pieces 18 are co-planar with the backside of the semiconductor die 12.

limitations from claim 25, and encapsulating the die with a body 22 such that, in fig. 4, the metallized backside of the die is adjacent a window defined within the body 56, col. 7, line 35-51;

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 18, 20, 24, 25 above, and further in view of Layher et al., U.S. Patent No. 4,678,358.

McShane does not specify using preplated leads, but Layher does. Layher teaches in figs. 1 and 2 forms lead frame 10 provided with preplated leads 11, p. 4, lines

25-41, and col. 2, line 47 - col. 3, line 10. Layher gives motivation in col. 2, lines 6-21. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Layher's process with McShane's invention would have been beneficial because the invention does not subject the parts to a working temperature that will diffuse or melt the coating.

Claims 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 18, 20, 24, 25 above, and further in view of Fosberry et al., U.S. Patent No. 6,214,640.

McShane does not specify using posts for attaching dies, but Fosberry does. Fosberry teaches in fig. 11, wherein the die 12 is coupled to the leadframe 22 die attach pad and post, col. 10, lines 16-57, via solder bumps (not shown), and wherein the solder bumps are reflowed, col. 15, line 53 - col. 16, line 38. Fosberry gives motivation in col. 2, lines 21-55. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Fosberry's process with McShane's invention would have been beneficial because the invention allows encapsulation without prefabricated support structure.

Claims 19, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 18, 20, 24, 25 above, and further in view of Merrill, U.S. Patent No. 5,654,206.

McShane does not specify the common use of transistors in his chips, but Merrill does. Merrill in fig. 1 shows semiconductor die 10 with boding pads 13 and 14, col. 2, lines 17-39, and in col. 1, lines 17-28 describes attaching the leads to power transistor and gate and source leads. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Merrill's process with McShane's invention would have been beneficial because the invention makes efficient connections between the transistors and the leads.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 18, 20, 24, 25 above, and further in view of Vasquez, et al., U.S. Patent No. 5,578,841.

McShane does not specify the forming a drain terminal on the backside, but Vasquez does. Vasquez teaches in fig. 1, the chip 17 wherein the backside forms a drain terminal 26 of a MOSFET in the die, col. 6, lines 26-36. Vasquez gives motivation on col. 6, lines 26-36. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Vasquez's invention with McShane's invention would have been beneficial because it reduces the overall die size.

Response to Arguments

Applicant's arguments with respect to claims 7-17 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 18-25 filed 6 December 2004 have been fully considered but they are not persuasive. Applicant argues McShane fails to teach limitiation, "the backside is substantially flush with the exterior surface of the molding compound" and that the examiner's interpretation is unreasonable.

Examiner respectfully disagrees. Examiner first alludes to claim 18, line 1, in which the applicant has stated that the claim is a 'comprising' one leaving any further features may be added to the claimed invention. Further in claims 25 and 26, the applicant adds more metal layers and structures to the backside of the die. McShane in fig. 4, cited above, shows the structure 54 exposed by the window 56. This structure 54 is a metal layer and attached to the chip. McShane also does not teach the thickness of the outer molding, instead sketching the thickness heuristically. The practitioner may optimize the thickness of the molding and therefore, the surface of 54 may appear to be "substantially flush" as enumerated by the claim. It is reminded that the examiner is duty bound to serve the public and thus to give claims their broadest reasonable interpretation.

Examiner must give claims their broadest reasonable interpretation, MPEP §2111, "During patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.' Applicant always has the opportunity to amend the claims during prosecution and broad interpretation by the

examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified, *In re Pratter*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969), *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997)." Also see *In re Zletz*, 13 USPQ 2d. 1320 (Fed. Cir. 1989).

For the above reasons, the rejection is considered proper.

Conclusion

For claims 7-17, 26:

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

For claims 18-25:

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

29 December 2004
WB

W. DAVID COLEMAN
PRIMARY EXAMINER